LT-Link Series Datasheet

Low-latency PCIe endpoint

Host interface: low-overhead PCIe endpoint profile.
Primary paths: command, telemetry, status, interrupt, and control registers.
Reference latency: 18 us median round trip, 44 us 99th percentile in test setup.
Core blocks: queue strategy, register map, interrupt handling, FPGA acknowledgement logic.
Primary use: deterministic control paths where bounded response time matters.
Support scope: endpoint profile, user-space API, latency test utilities.